

5432 Zotino

Features

- 32-channel DAC.
- 16-bits resolution.
- 1 MSPS shared between all channels.
- Output voltage ± 10 V.
- HD68 connector.
- Can be broken out to BNC/SMA/MCX.

Applications

- Controlling setpoints of PID controllers for laser power stabilization.
- Low-frequency arbitrary waveform generation.
- Driving DC electrodes in ion traps.

General Description

The 5432 Zotino is a 4hp EEM module part of the AR-TIQ Sinara family. It adds digital-analog converting capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

It provides 4 groups of 8 analog channels each, exposed by 1 HD68 connector. Each channel supports output voltage from -10 V to 10 V. All channels can be updated simultaneously. Channels can broken out to BNC, SMA or MCX by adding external 5518 BNC-IDC, 5528 SMA-IDC or 5538 MCX-IDC cards.

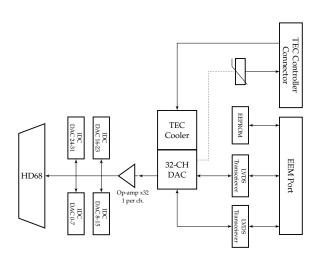


Figure 1: Simplified Block Diagram



Figure 2: Zotino Card photo

Electrical Specifications

The specifications are based on the datasheet of the DAC IC (AD5372BCPZ¹), and various information from Sinara wiki².

Parameter	Min.	Тур.	Max.	Unit	Conditions
Output voltage	-10		10	V	
Output impedance ²	470 Ω 2.2nF				
Resolution ¹		16		bits	
3dB bandwidth ²		75		kHz	
Power consumption ²	3		8.7	W	

Table 1	1:	Output	Specifications
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The following are cross-talk and transient behavior of Zotino³. In terms of output noise, it was measured after 15 cm IDC cable, IDC-SMA, 100 cm coax (\sim 50 pF), and 500 k $\Omega \parallel$ 150 pF⁴. The DAC output during noise measurement is 3.5 V.

Parameter	Min. Typ.	Max.	Unit	Conditions / Comments
DC cross-talk ³	-116		dB	
Fall-time ³	18.5		$\mu \mathbf{s}$	10% to 90% fall-time
	25		$\mu \mathbf{s}$	1% to 99% fall-time
Negative overshoot ³	0.5%		-	
Rise-time ³	30		$\mu \mathbf{s}$	1% to 99% rise-time
Positive overshoot ³	0.65%		-	
Output noise ⁴				
@ 100 Hz	500		nV/rtHz	6.9 Hz bandwidth
@ 300 Hz	300		nV/rtHz	6.9 Hz bandwidth
@ 50 kHz	210		nV/rtHz	6.9 kHz bandwidth
@ 1 MHz	4.6		nV/rtHz	6.9 kHz bandwidth
> 4 MHz		1	nV/rtHz	6.9 kHz bandwidth

Table 2: Electrical Characteristics

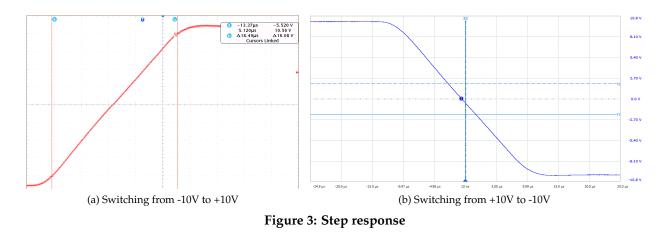
¹https://www.analog.com/media/en/technical-documentation/data-sheets/AD5372_5373.pdf

²https://github.com/sinara-hw/Zotino/wiki

³https://github.com/sinara-hw/Zotino/issues/21

⁴https://github.com/sinara-hw/Zotino/issues/27

Step response are found by setting the DAC register to 0x0000 (-10V) or 0xFFFF (10V) and observe the waveform³.



Far-end crosstalk is measured using the following setup³.

- 1. CH1 as aggressor, CH0 as victim
- 2. CH0, 2-7 terminated, CH 8-31 open
- 3. Aggressor signal from BNC passed through 15cm IDC26, 2m HD68-HD68 SCSI-3 shielded twisted pair, 15cm IDC26, converted back to BNC with adapters between all different cables & connectors.

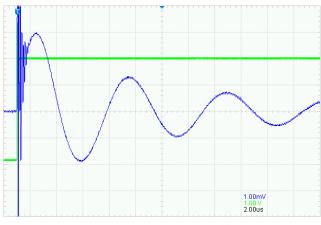


Figure 4: Step crosstalk

Front Panel Drawings

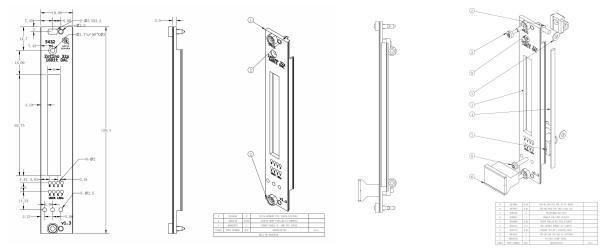


Figure 5: 5432 Zotino front panel drawings.

Example ARTIQ code

The sections below demonstrate simple usage scenarios of the 5432 Zotino card with the ARTIQ control system. They do not exhaustively demonstrate all the features of the ARTIQ system. The full documentation for the ARTIQ software and gateware is available at https://m-labs.hk.

Set output voltage

The following example initializes the Zotino card, then emits 1.0 V, 2.0 V, 3.0 V and 4.0 V at channel 0, 1, 2, 3 respectively. Voltages of all 4 channels are updated simultaneously with the use of $set_dac()$.

```
def prepare(self):
    self.channels = [0, 1, 2, 3]
    self.voltages = [1.0, 2.0, 3.0, 4.0]

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.zotino.init()

    delay(1*ms)
    self.zotino.set_dac(self.voltages, self.channels)
```

Triangular Wave

A triangular waveform at 10 Hz, 16 V peak-to-peak. Timing accuracy of the RTIO system can be demonstrated by the precision of the frequency.

```
from scipy import signal
import numpy
def prepare(self):
    self.period = 0.1 * s
    self.sample = 128
    t = numpy.linspace(0, 1, self.sample)
    self.voltages = 8*signal.sawtooth(2*numpy.pi*t, 0.5)
    self.interval = self.period/self.sample
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.zotino.init()
    delay(1*ms)
    counter = 0
    while True:
        self.zotino.set_dac([self.voltages[counter]], [0])
        counter = (counter + 1) % self.sample
        delay(self.interval)
```

Ordering Information

To order, please visit https://m-labs.hk and select the 5432 Zotino in the ARTIQ Sinara crate configuration tool. The card may also be ordered separately by writing to mailto:sales@m-labs.hk.

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